

FIG. 1

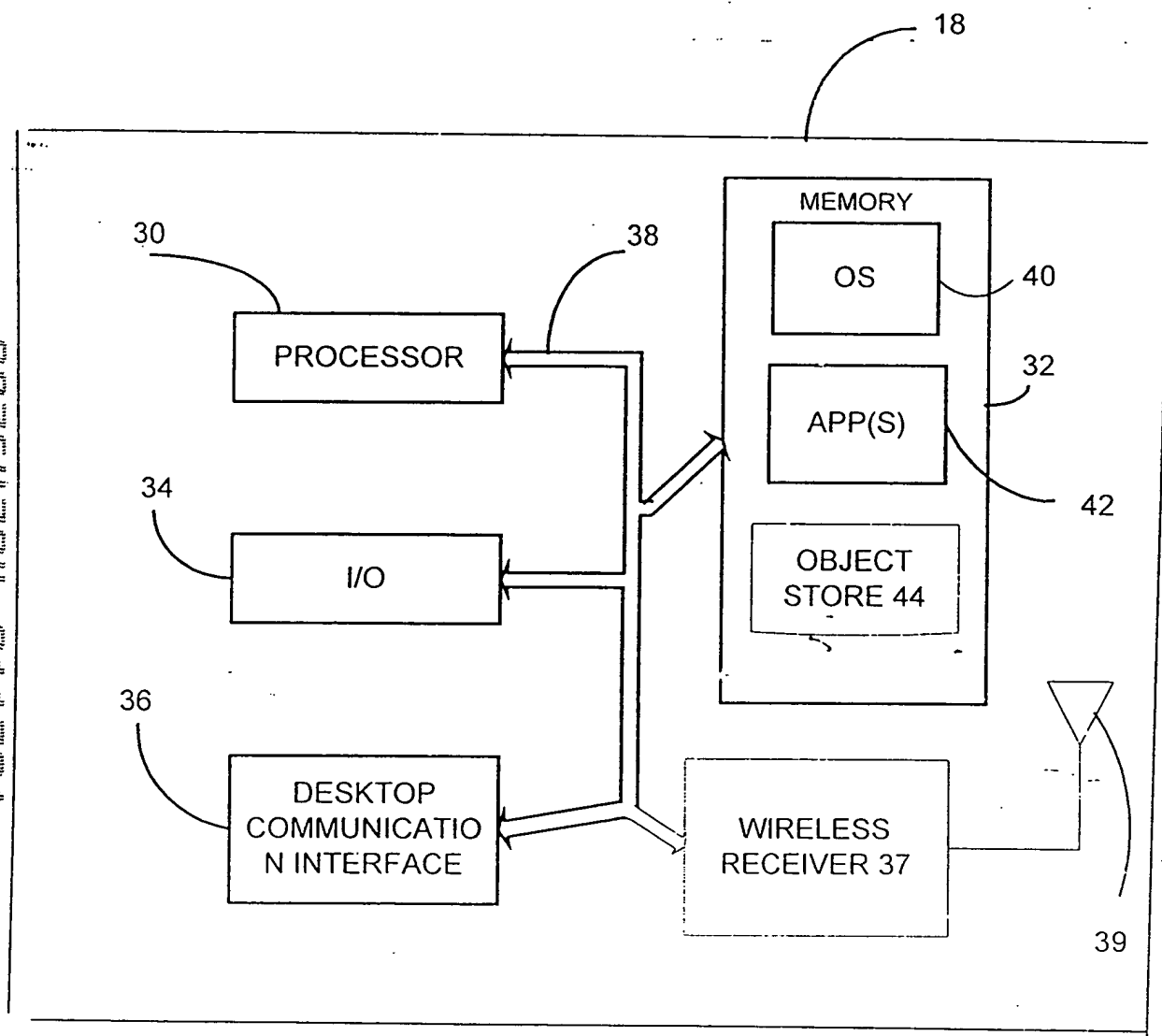


FIG.2

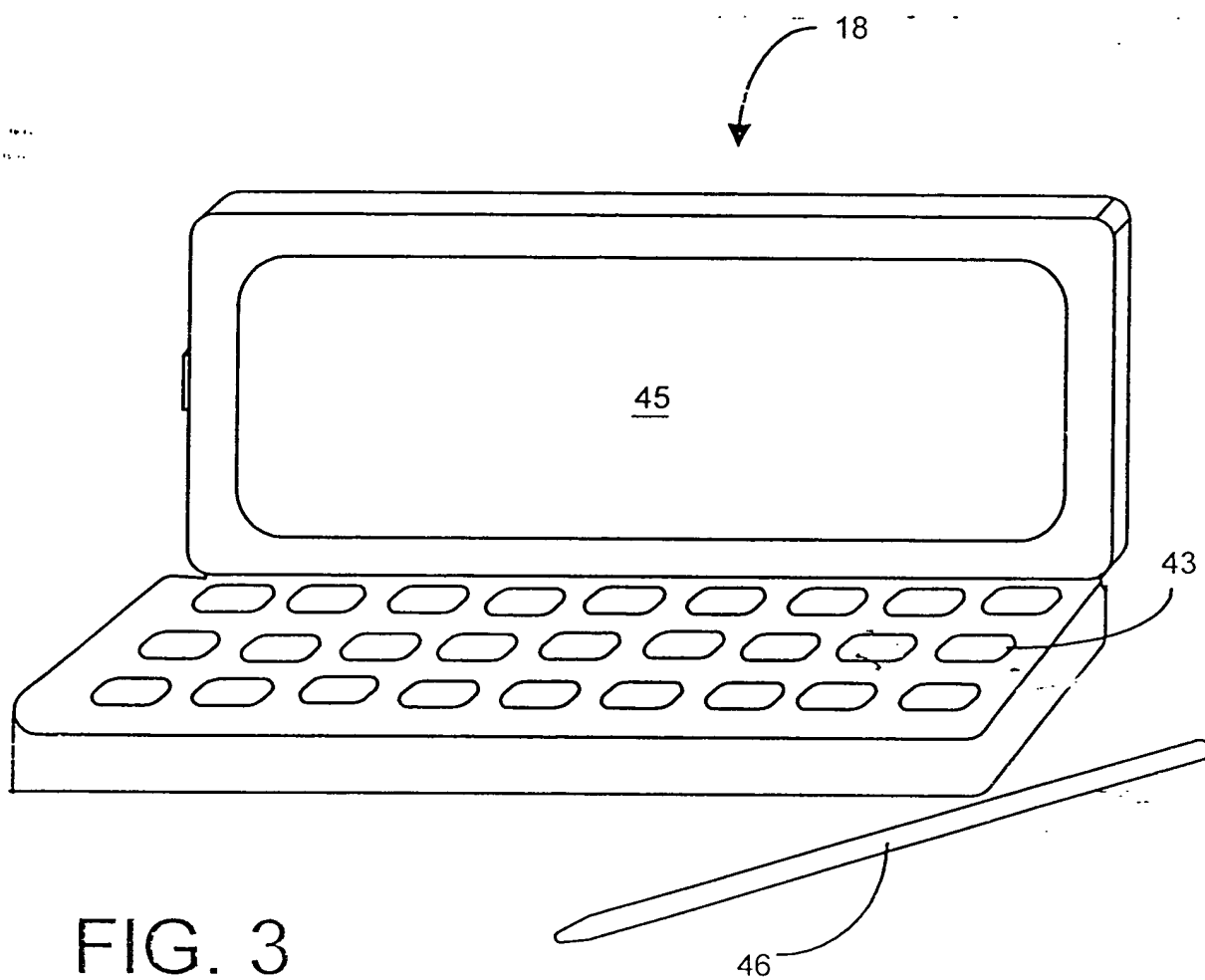


FIG. 3

FIG. 4 is a schematic diagram of a device 10 in a closed position.

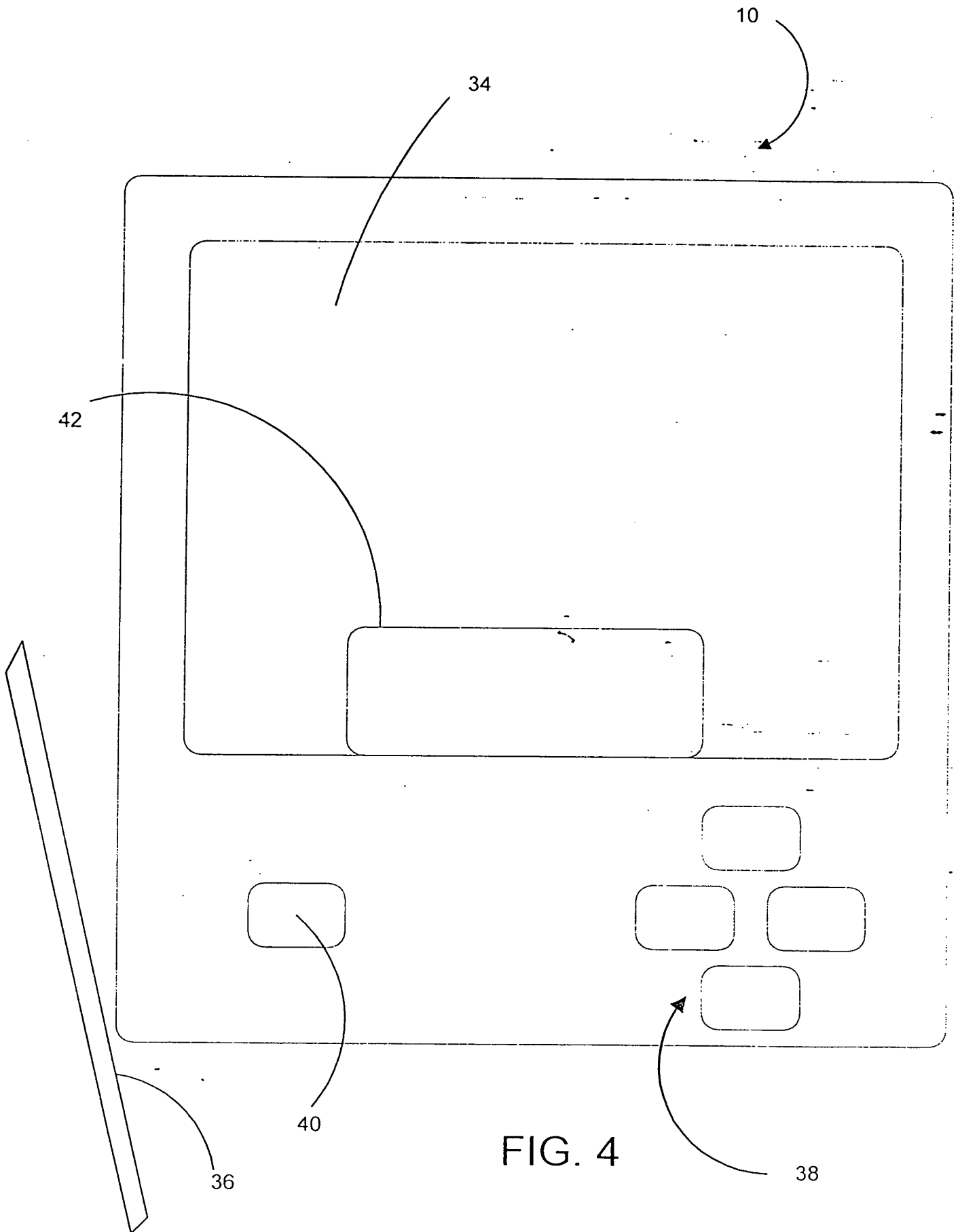


FIG. 4

FIG. 5

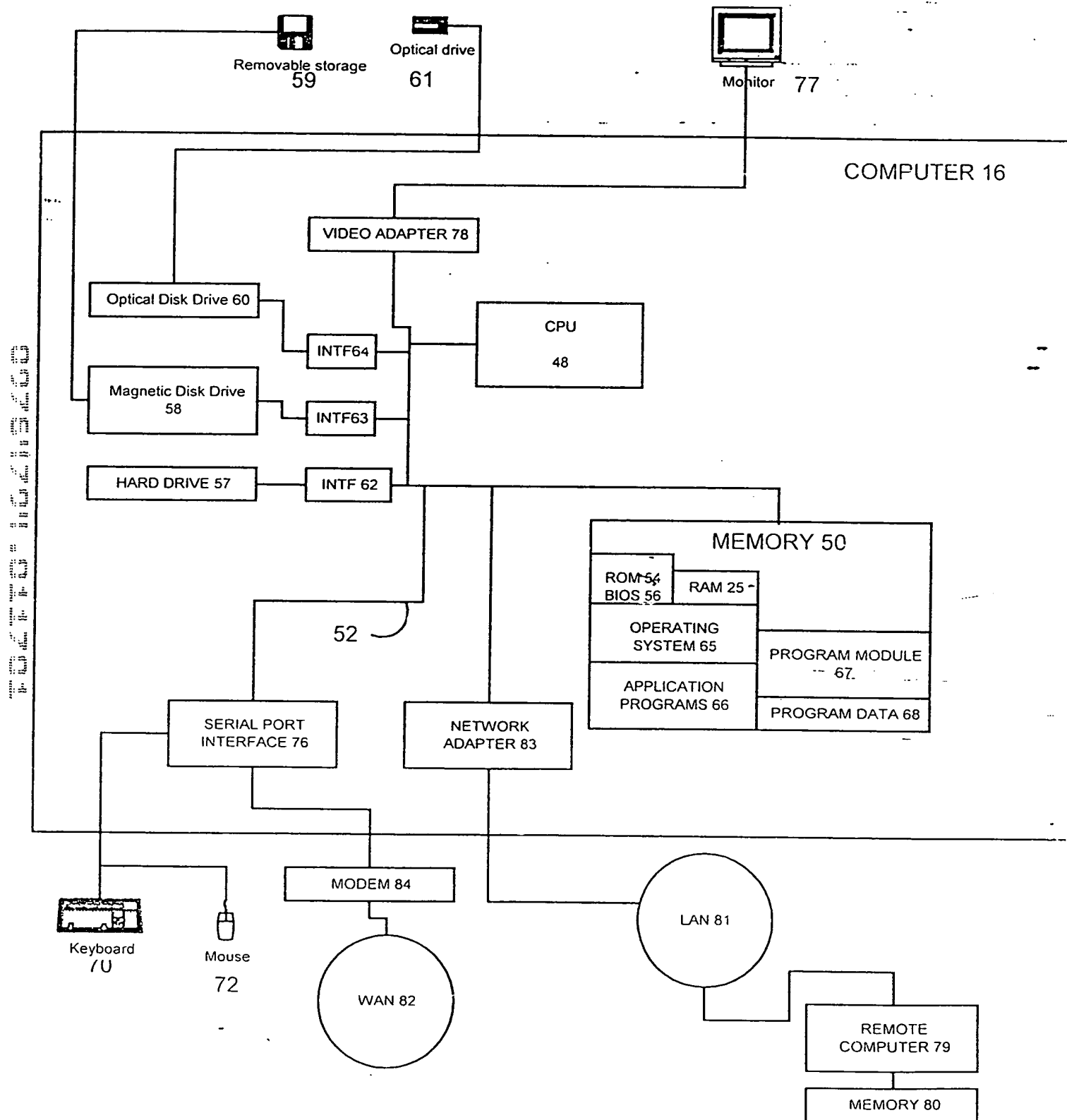
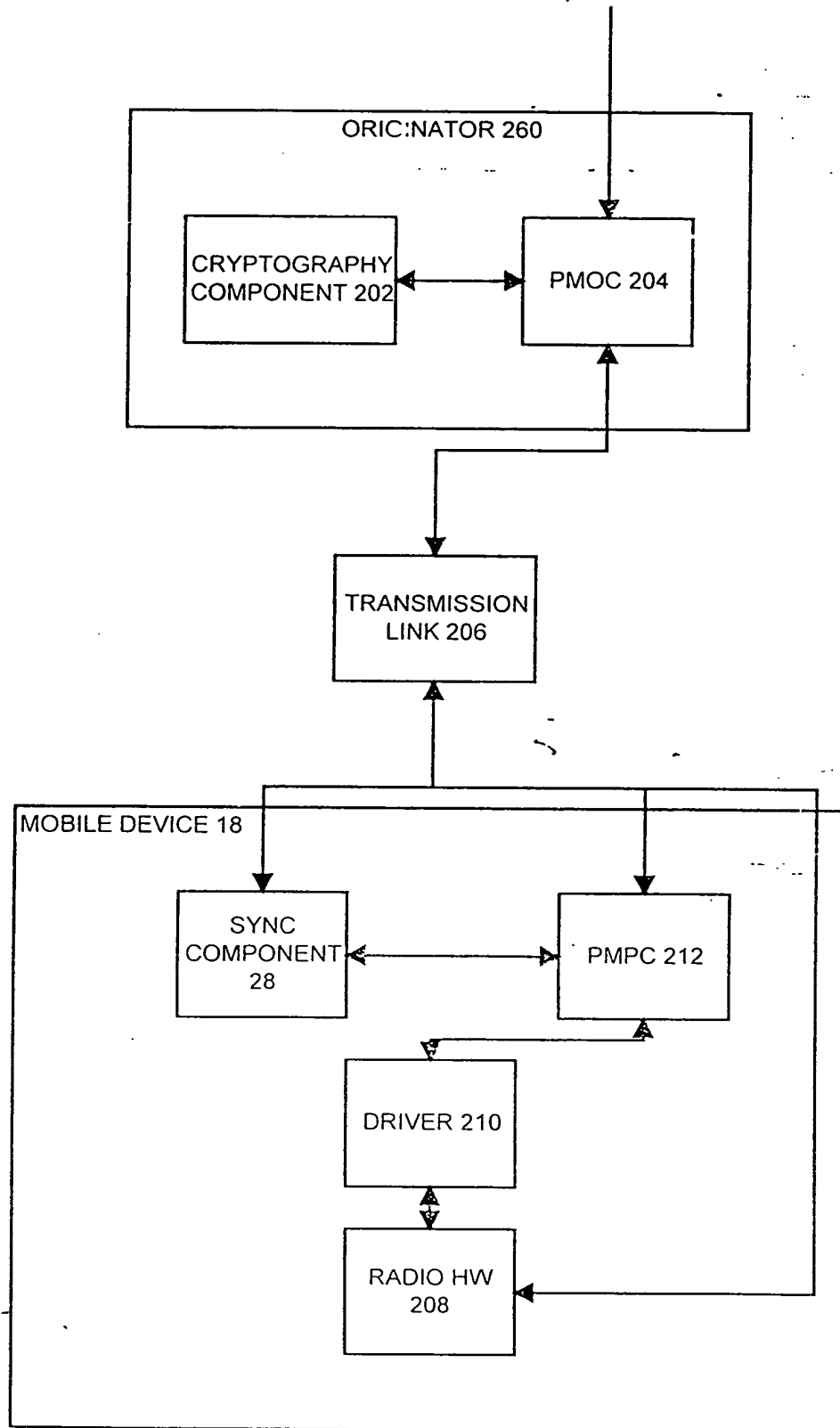


FIG. 6

PROGRAMMING DATA



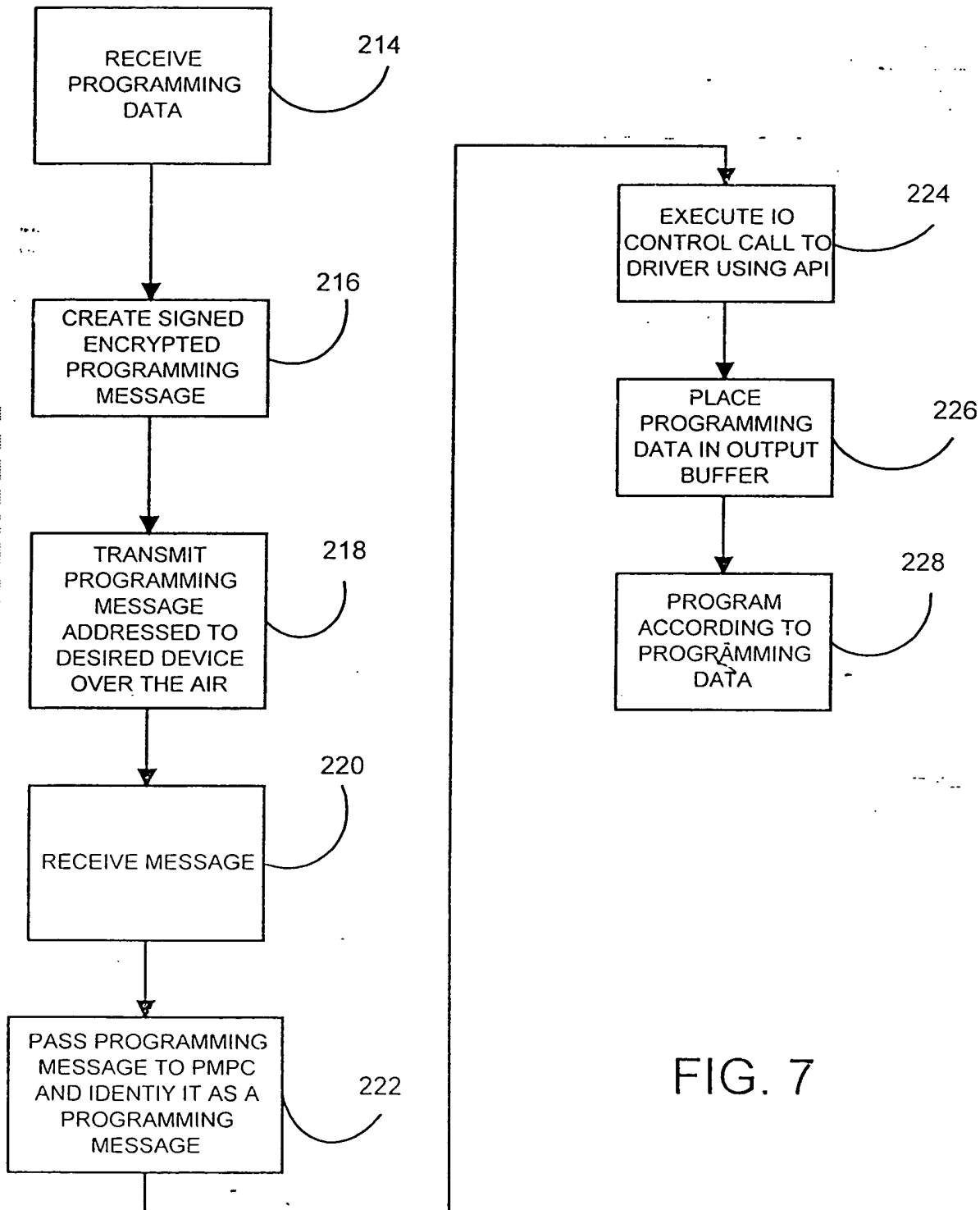


FIG. 7

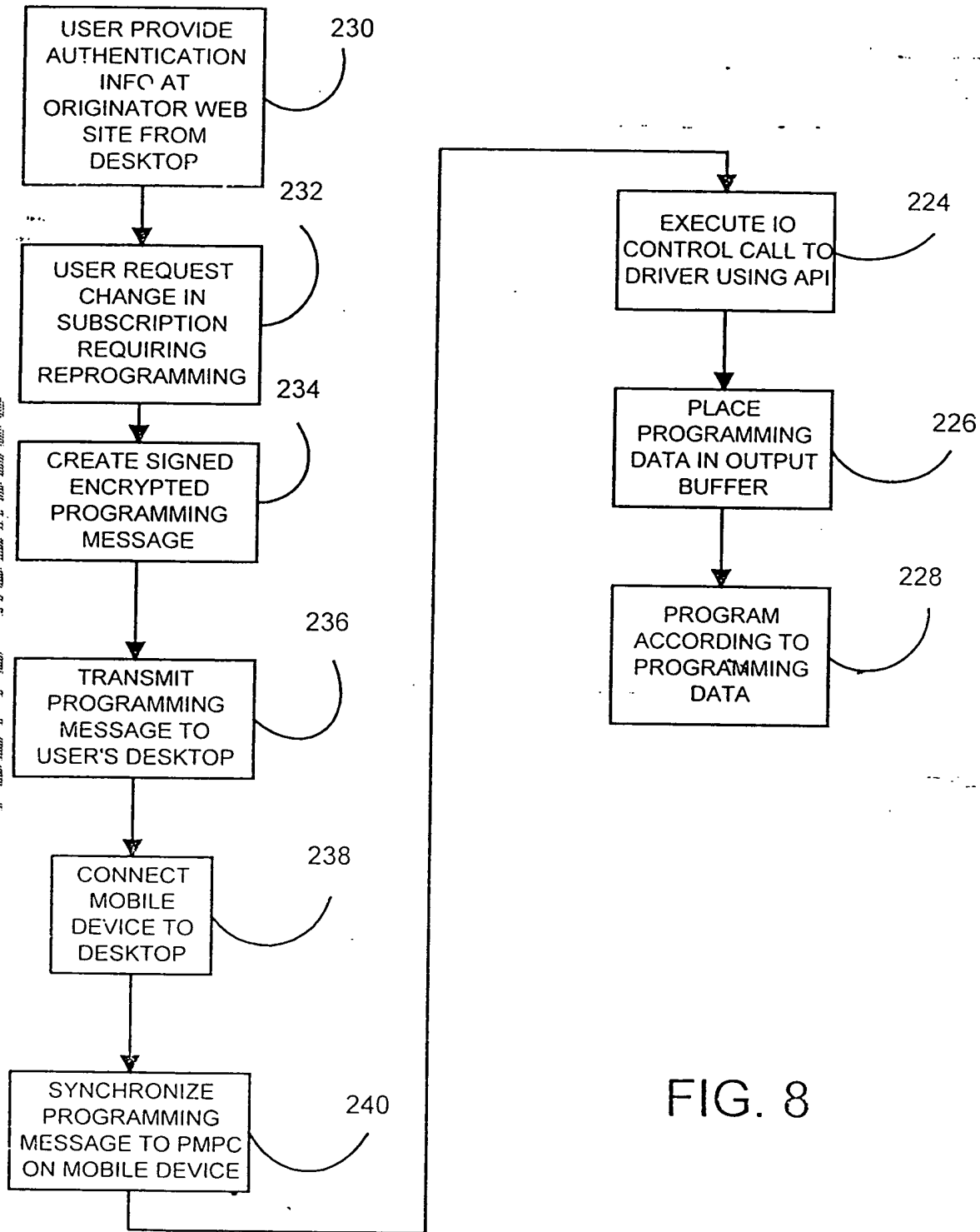
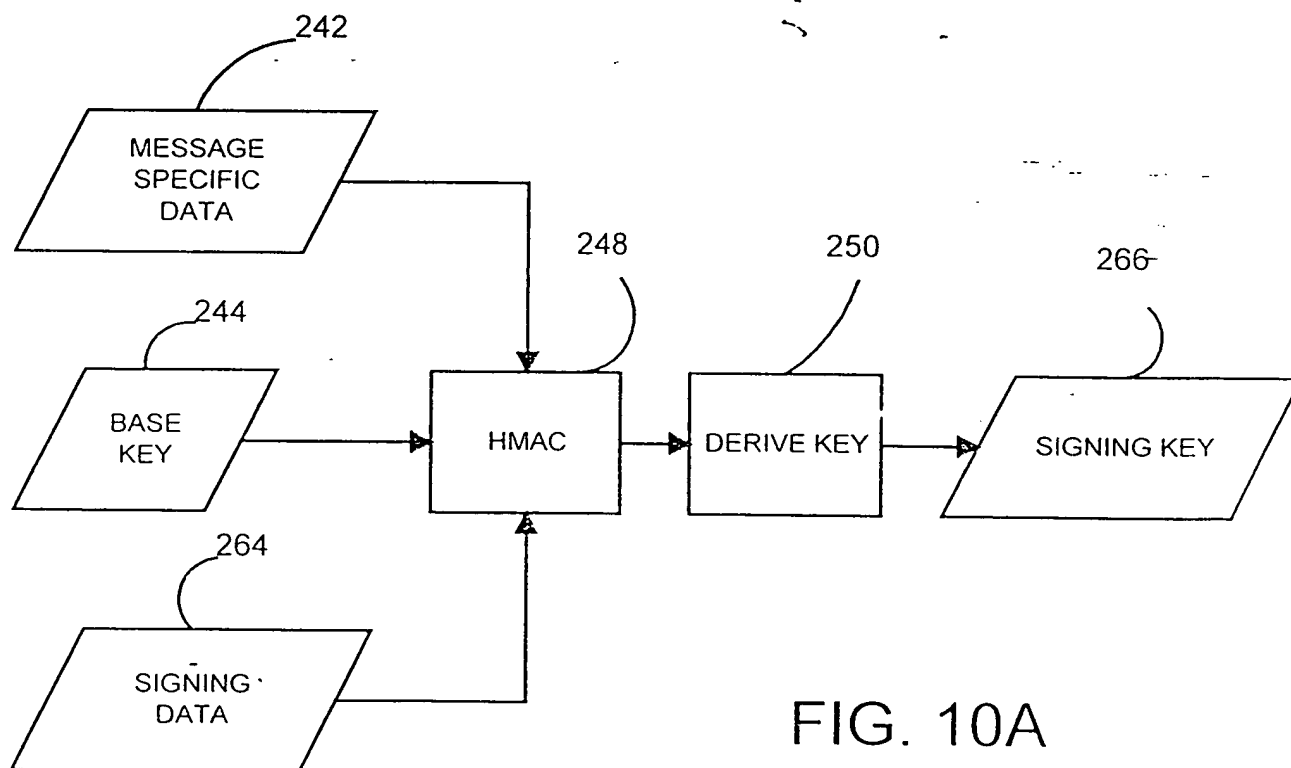
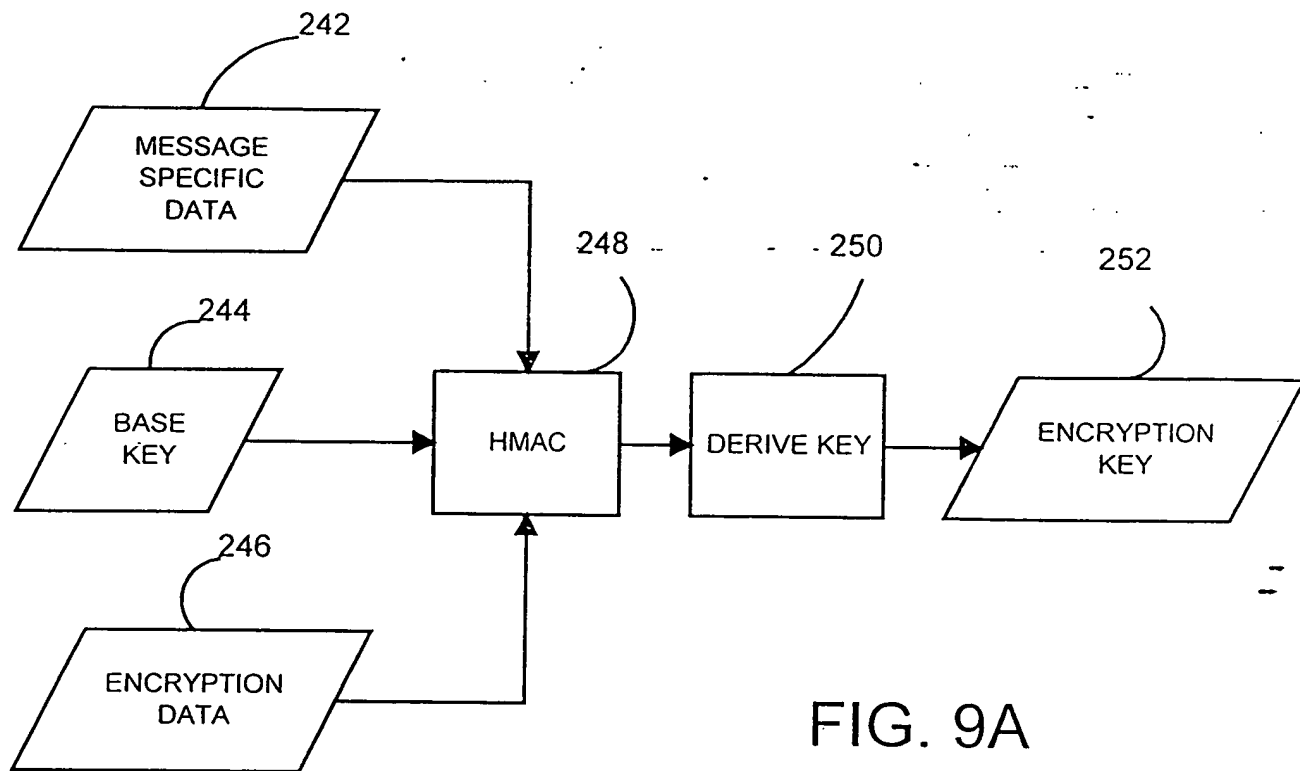


FIG. 8



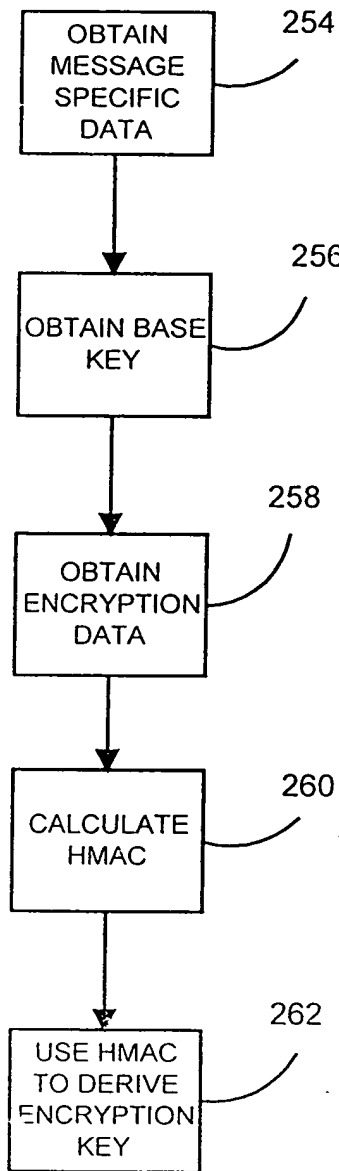


FIG. 9B

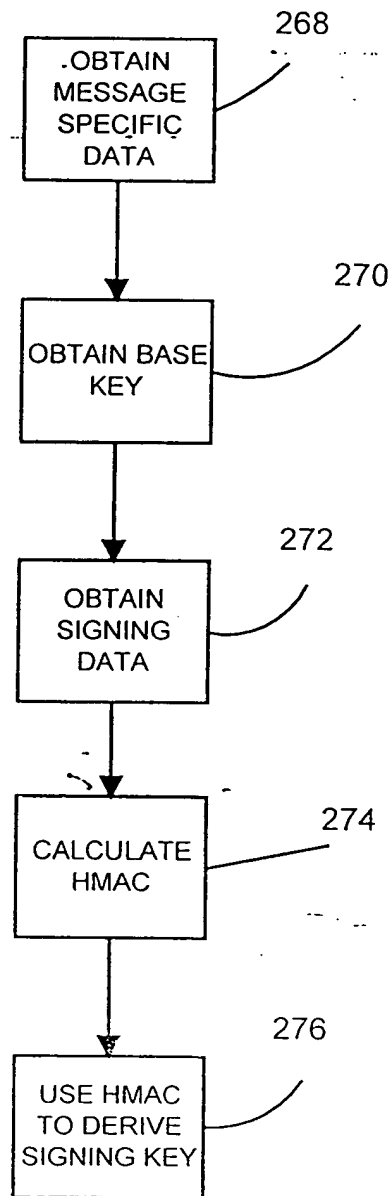
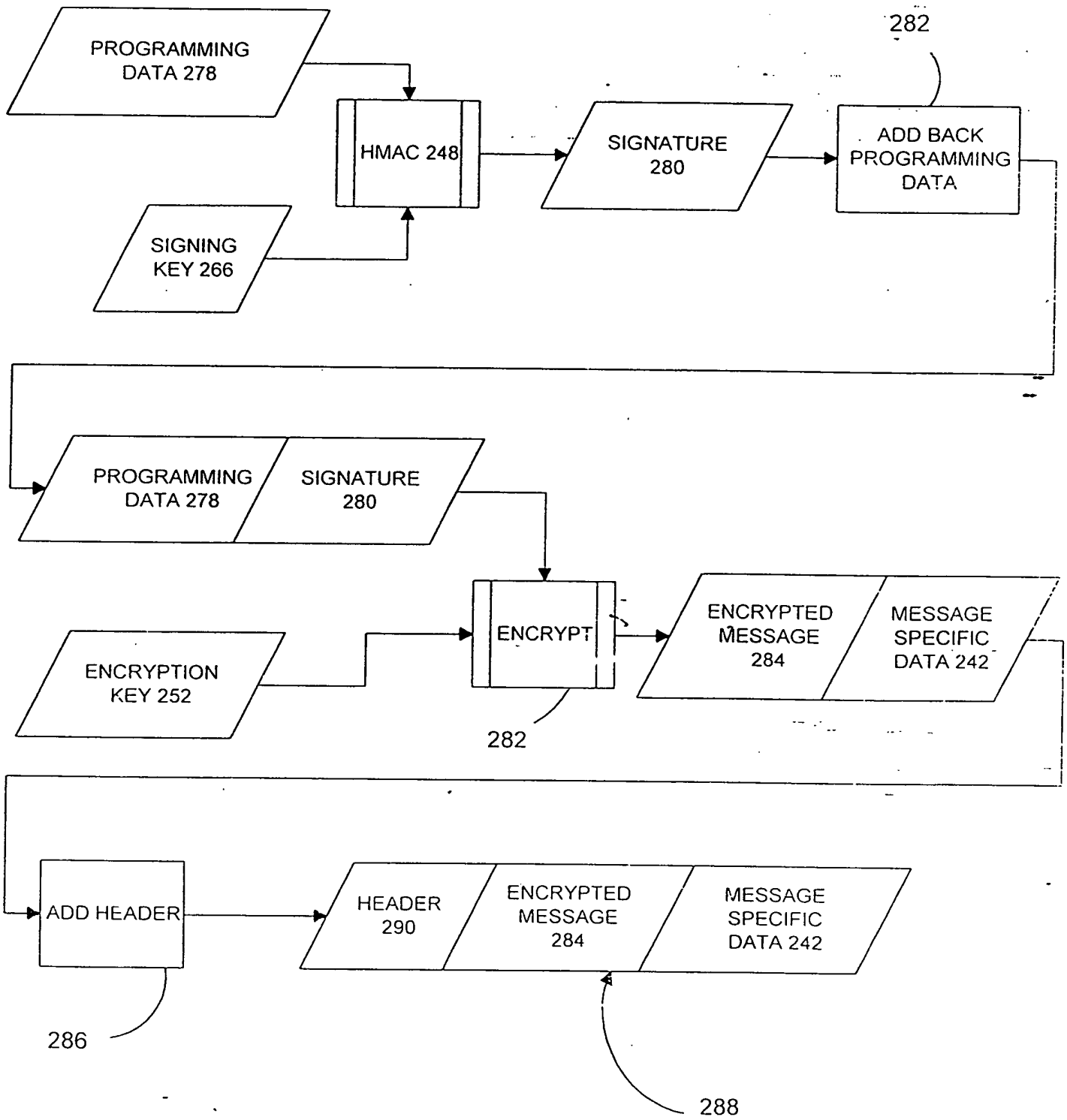


FIG. 10B

FIG. 11A



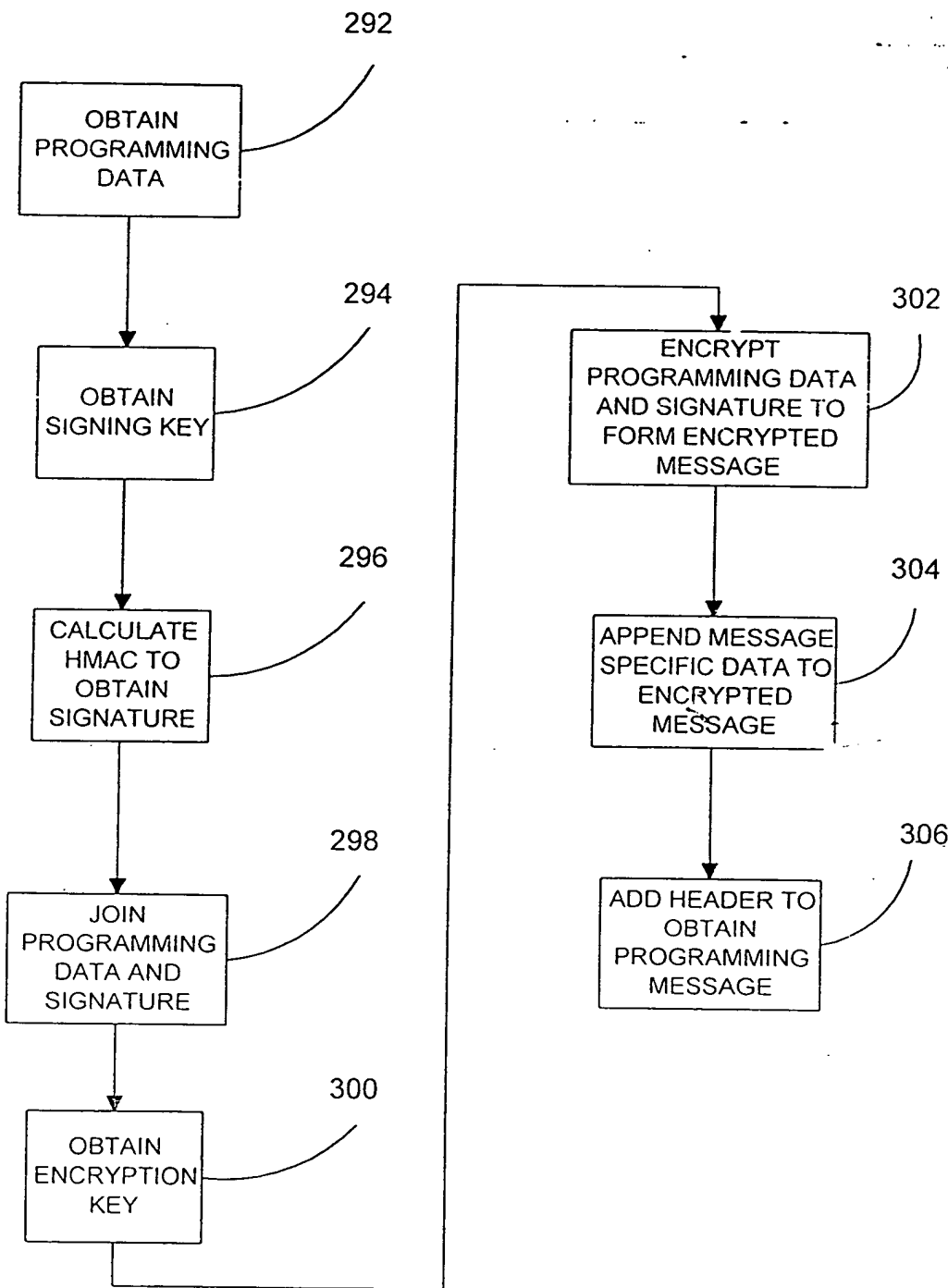
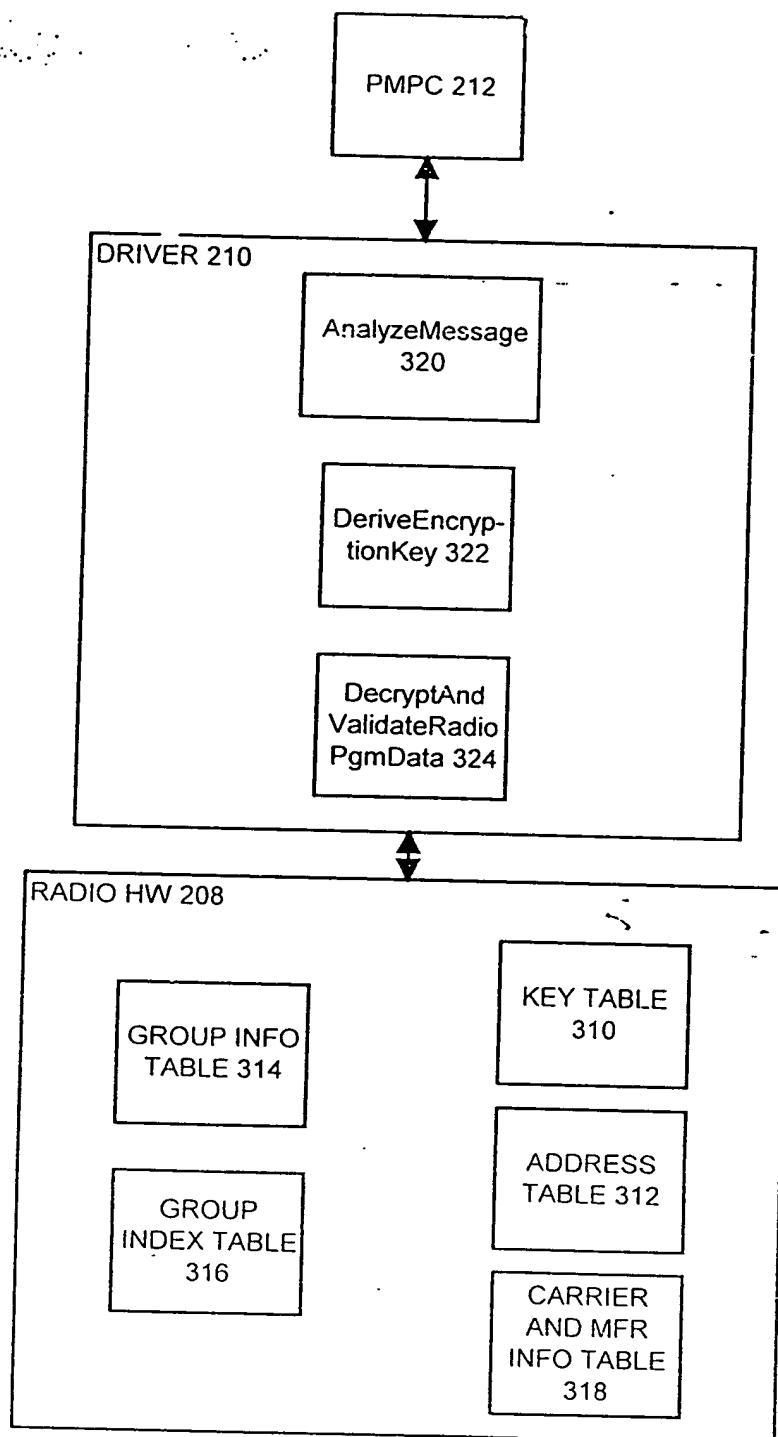


FIG. 11B

FIG. 12A



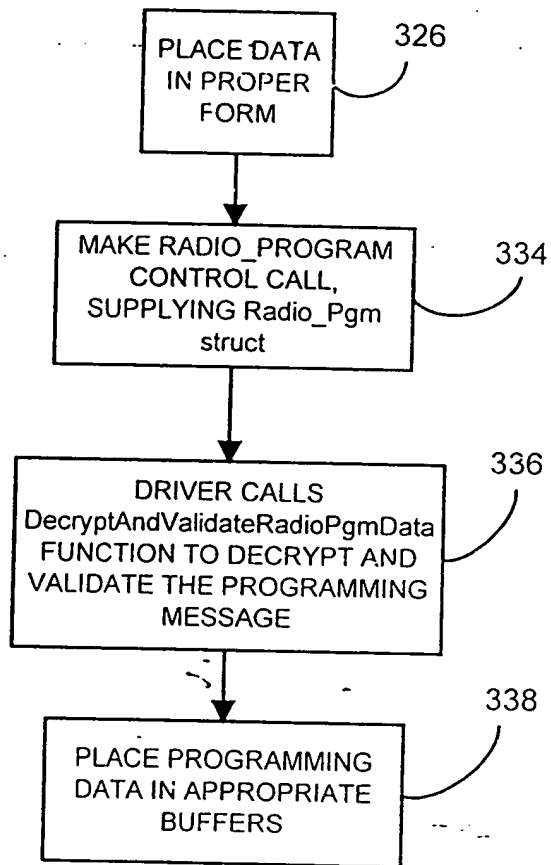


FIG. 12B